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Application Note

TELEVISION HORIZONTAL APC/AFC LOOPS: THE LAST 10 PERCENT

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A discussion of some common problems that may be encountered with the design of Horizontal APC/AFC loops and methods to avoid or overcome them.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

The design theory for modern television horizontal phase-locked loops is well understood (Reference 1) and, given reasonably linear circuit elements, the receiver designer can expect his APC loop to work pretty much as he designed it. If fact, it will appear that he has accomplished the bulk of the work when satisfactory pull-in range, and static and dynamic phase performance are obtained. This is usually a good time to pass the design from R & D to Production Engineering for the final 10 percent of the work to be done – and oddly enough, this last 10 percent can take just as long as the first 90 percent. Even with circuits that have excellent phase detector linearity (μ), and constant oscillator sensitivity (β) several defects can be apparent in the nearly finished design. These can include top-hook, push out, asymmetry of pull-in, flag waving and loss of sync at weak signal levels. This note describes these phenomena and presents ways of avoiding them or minimizing their visibility.

TOP-HOOK:

A congenital deformity of television phase-locked loops. It is usually manifested as a bend in vertical lines at the top of the television picture. The degree of bending and visibility of top hook depends on the relative recovery speed of the APC loop and the amount of vertical overscan. Frequently, interaction of the horizontal and vertical oscillator output stages, the effects of pin cushion correction, or picture phasing, can mask or enhance the top-hook . . . but it is always there.

To understand why top-hook is always present in television APC loops, we must be aware of two things:

1. During the vertical blanking period, the duration of the line sync pulses is cut in half from the normal 4.7 μs.

For the standard television signal (with negative polarity sync pulses) the leading edges of all line sync pulses are 63.5 μs apart. However, during the three line periods before and after the field sync pulse, the line pulse duration is only 2.3 μs and equalizing pulses of similar duration are added in the middle of the line period. The odd and even field blanking periods are compared to the line pulse timing in the photo and timing diagrams of Figure 1 (not to scale).

2. Television APC loops always synchronize to the mean sync pulse position.

Because of the need to generate correction signals of either polarity, the phase detectors are designed to give zero net output when phased at the center of the sync pulse. This is true for detectors gated by the sync pulse (MC1391/94 types) as well as for detectors using the syncs as a clamping pulse train (dual-diode bridge types).

The significance of this second point becomes obvious when it is realized that the mean position of the line sync pulses during the vertical blanking period occurs 1.2 μs early because of the reduced pulse width. A phase-locked loop will operate during this period to shift phase to the new mean pulse position, causing the picture to be displaced to the right hand side at the top of the raster. After the vertical blanking period, the phase detector will return to phasing at the center of the wider line sync pulses and the recovery time necessary to do this causes the picture displacement (or top-hook) to be visible.

As mentioned earlier, the visibility of top-hook can vary a great deal. If the APC loop has an extremely slow response to a phase change, little shift in the picture position will occur during vertical retrace and correspondingly little need to recover during scan time. Conversely, if the APC loop is extremely fast, the picture will displace the full 1.2 μs and the recovery is equally rapid. As the vertical is usually overscanned to some degree, again the recovery may not be visible. Unfortunately, neither of these two cases represent satisfactory loop designs since these extreme response characteristics will produce poor airplane flutter performance or poor impulse noise immunity respectively. In general, optimum APC loop transient response will be such as to allow top-hook to be visible.

Top-hook can be clearly demonstrated and observed by modifying a television receiver to phase advance the horizontal sweep by about 25 μs and the vertical sweep by about 4 ms (suitable circuits to do this are shown in Appendix C. Note that although phase delay of the vertical sync is used, the horizontal is phase adjusted by delaying the sawtooth reference to the phase detector. Also, since the AGC system is usually gated from the horizontal sweep, either sync gating or a battery bias must be used to control the gain of the RF and IF amplifiers). With proper adjustment of the brightness and contrast controls, this results in the horizontal and vertical blanking periods being visible on the picture tube.

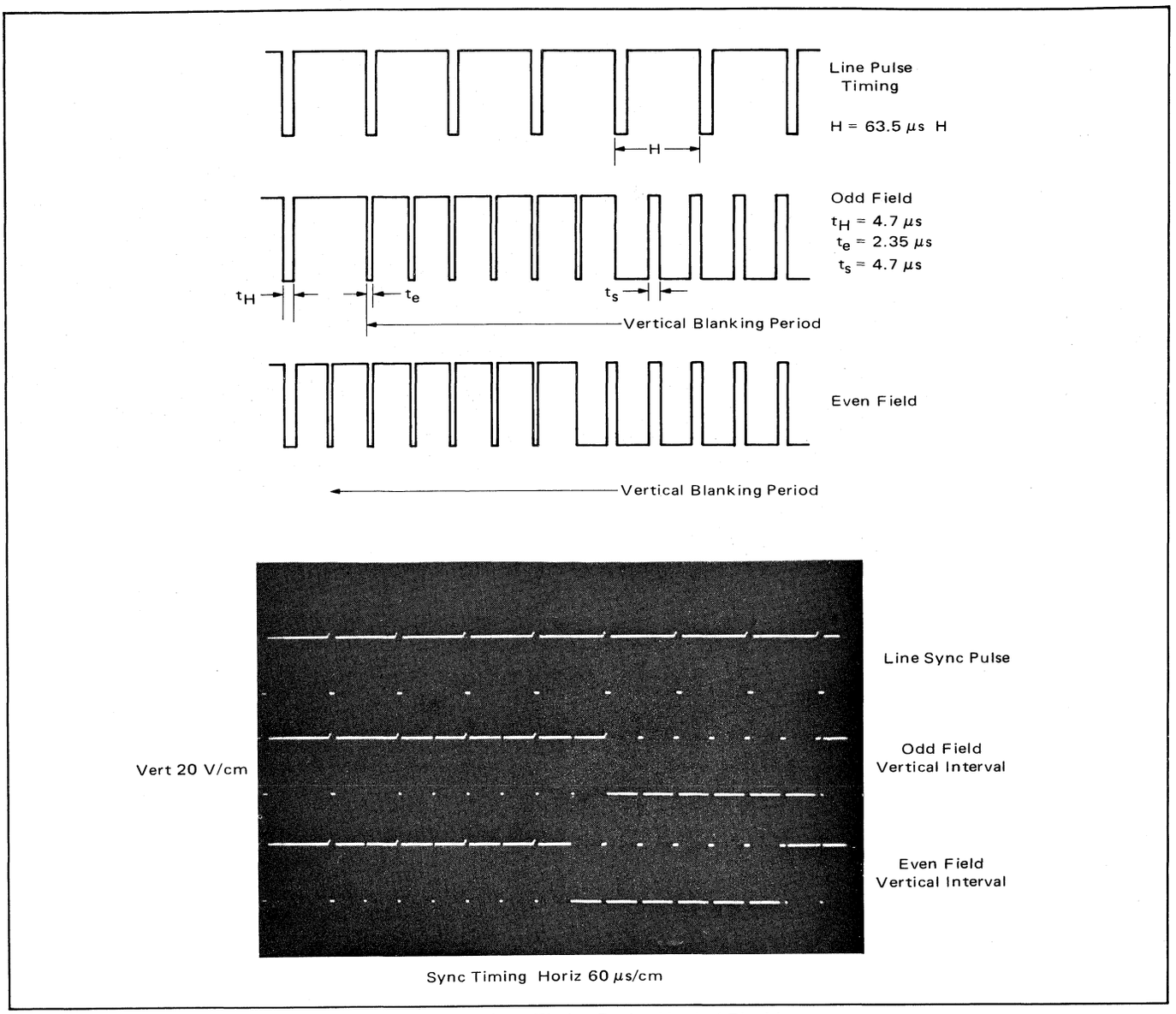


FIGURE 1 – Sync Timing During Vertical Blanking

Figure 2 shows the response of a typical APC loop during the vertical blanking period (2a), and the video waveform corresponding to section x-x of the blanking period (2b) (this waveform is idealized in Figure 2d). From the close-up view of the vertical blanking period in 2c it can be seen that during the three line periods preceding the vertical sync pulse, the APC loop is clearly attempting to recenter the narrow line sync pulses to the center position of the wide line sync pulse. By the end of the vertical blanking period, the phase of the line sync pulses is almost 1.2 μs to the right, resulting in the following video information at the top of the screen, appearing bent to the right.

Interestingly, during the three line periods occupied by the serrated field sync pulse, the phase detector is attempting to shift the picture in the opposite direction – to the left. The reason for this is the location of the sync pulses with respect to the reference sawtooth waveform derived from the horizontal flyback pulse. Figure 3 compares the timing of the syncs and the sawtooth and assumes, for the moment, that the line sync pulses are centered at the mid-point of the steep portion of the sawtooth. A normal width line sync pulse produces a net zero correction signal. The narrow line sync pulse produces a net positive correction signal, phase delaying the picture information. The serrated field pulse produces a net negative correction signal tending to phase advance the picture information on the picture tube. Note that only the area within the confines of the steep portion of the sawtooth is considered since this is the stable operating region of the APC loop. Outside this region, the loop gain is much lower and reversed in polarity (Reference 2).

Having discussed the origin of top-hook in some detail, we can now direct our attention to avoiding it or minimizing the effect – short of petitioning the F.C.C. to change the sync timing during the vertical blanking period.

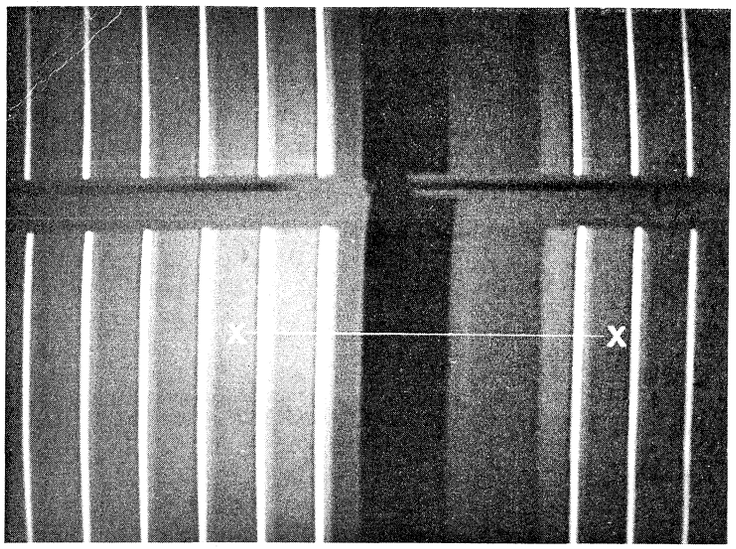


FIGURE 2a – Sync Blanking Periods
Picture tube with video pattern of vertical white lines.
Video delayed to show blanking intervals.

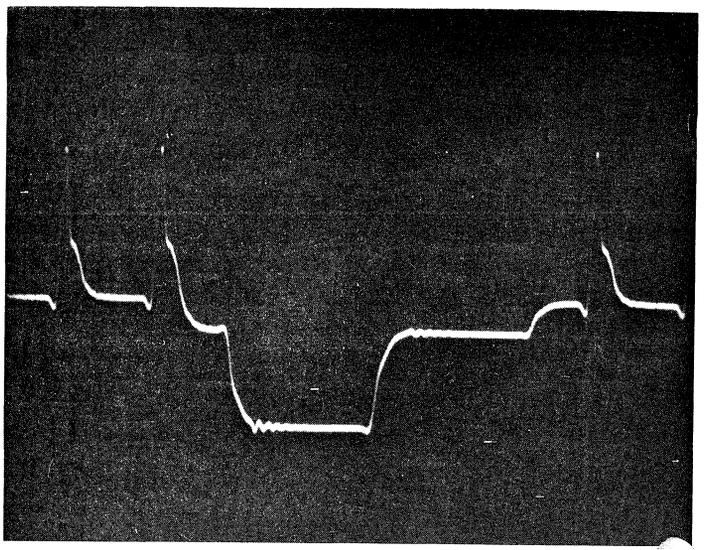


FIGURE 2b – Video Detector Output Corresponding to Section X-X on 2a

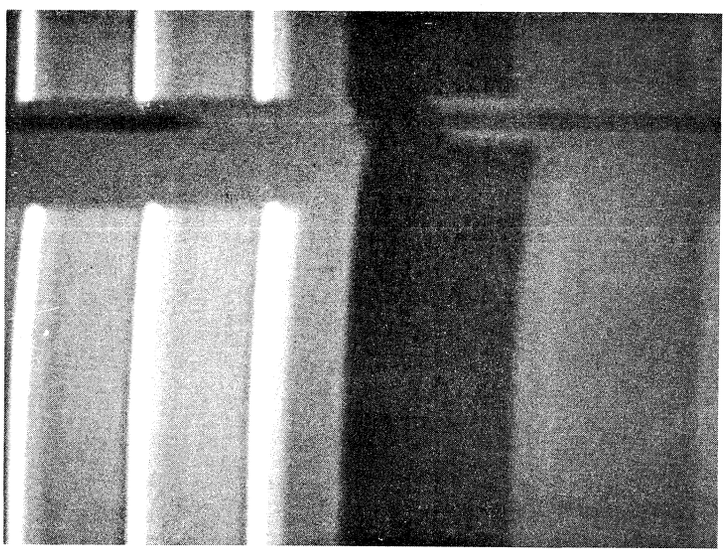


FIGURE 2c – Vertical Blanking Interval
Close-up view of vertical blanking period shown in 2a.

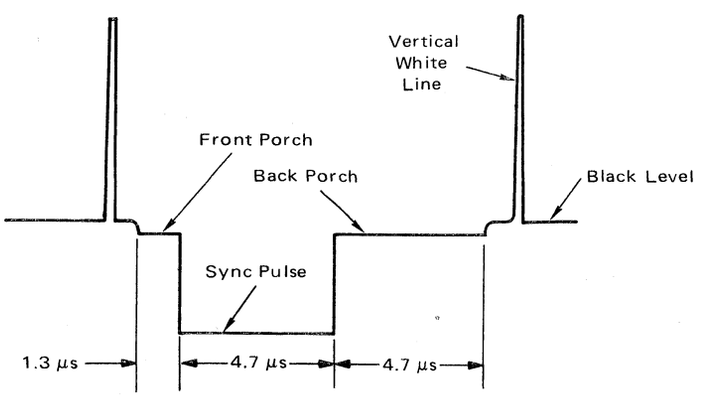
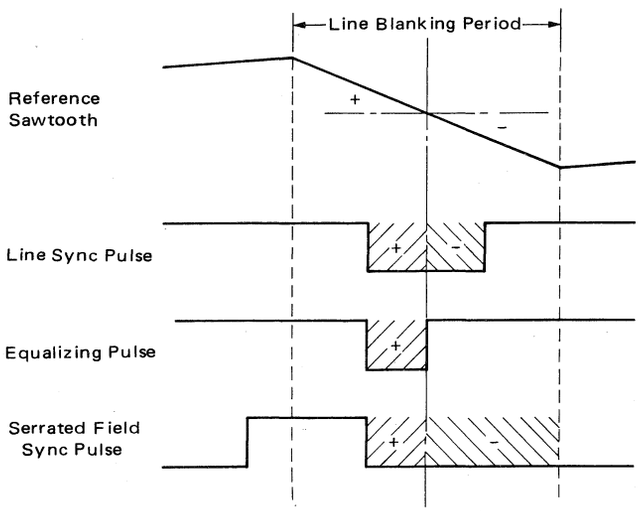
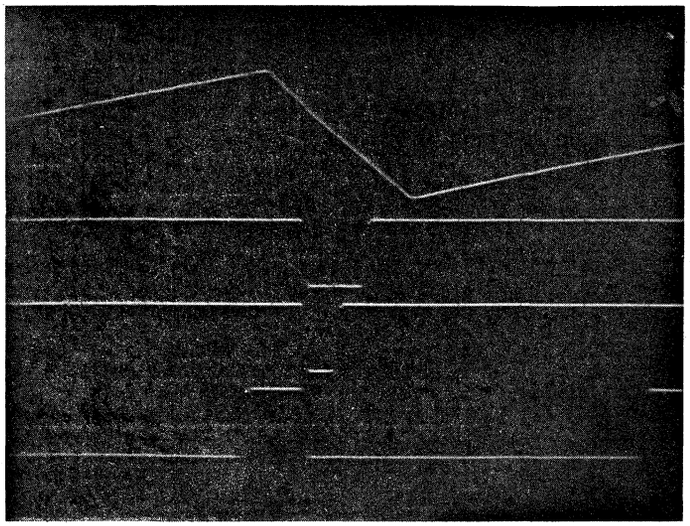


FIGURE 2d – Horizontal Blanking Period



The Symbols + - Refer to the Polarity of a MC1394 Phase Detector Current with the Timing Relationships Shown



Horizontal 6 μs/cm

Sync/Sawtooth Timing

FIGURE 3 – Sync/Sawtooth Timing

Since the phase detector synchronizes the oscillator to the mean pulse position, one solution is to reduce the line pulses and the serrated vertical pulse to the same width as the equalizing pulses (2.3 μs). A simple way to do this is to differentiate the sync pulses and a typical network is shown in Figure 4. With the component values given, a line pulse will appear as shown in Figure 5, the solid line indicating the bias level at which the MC1391/94 phase detector is gated on. Similarly, the equalizing pulses and the serrated vertical pulse will appear as shown in Figure 6, all pulses now being effectively 2.3 μs wide at the phase detector input. Figure 7 shows that this removes horizontal phase shifts during the vertical blanking period. An important point with sync differentiation is to ensure that a low sync source impedance is used. If this is not the case, flag waving (discussed later) can result.

This method, while simple, is not without penalty. For a dual diode bridge the energy of the clamping pulses is reduced and could result in a loss of phase detector sensitivity. For gated-phase detectors for MC1391/94 type, although the phase detector sensitivity is independent of the pulse width, the linear operating region is reduced (see Appendix A) and during large phase transients, the ability of the detector to charge or discharge the filter capacitors becomes decreased. This effect is clearly shown in Figure 8, depicting the phase detector response to a 3 μs delay in the signal produced by a jitter generator. In the case of the reduced pulse width system, the recovery time from the phase transient is appreciably longer.

Another technique for minimizing the effects of top-hook is to take advantage of the phase offset produced in the opposite direction by the serrated vertical pulse. This

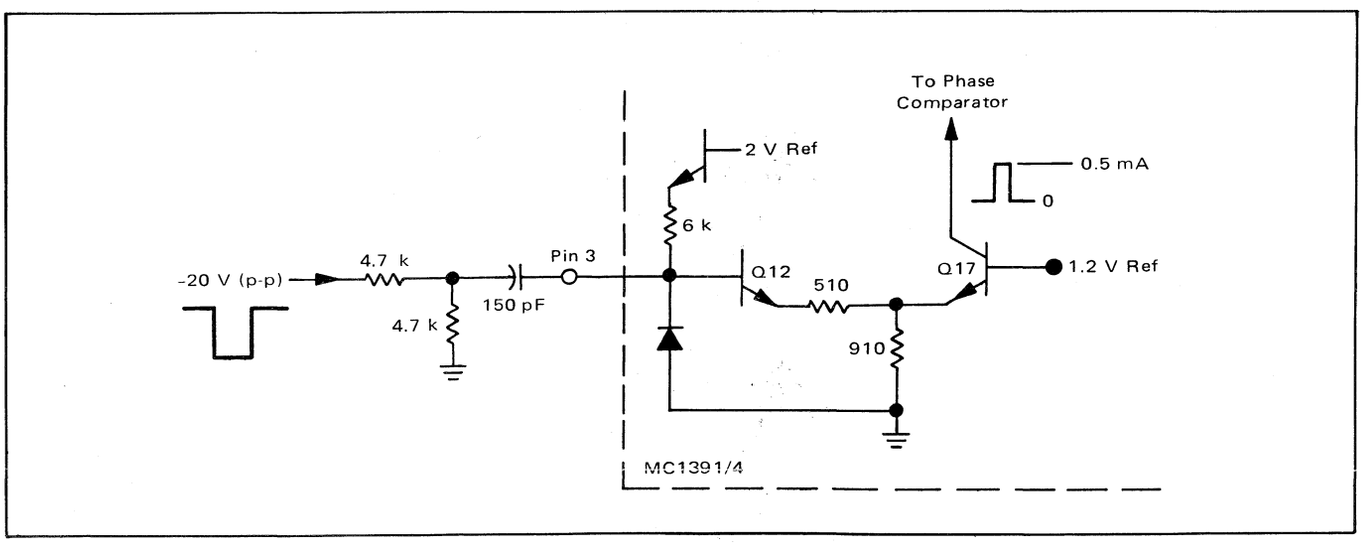


FIGURE 4 – Sync Pulse Differentiation

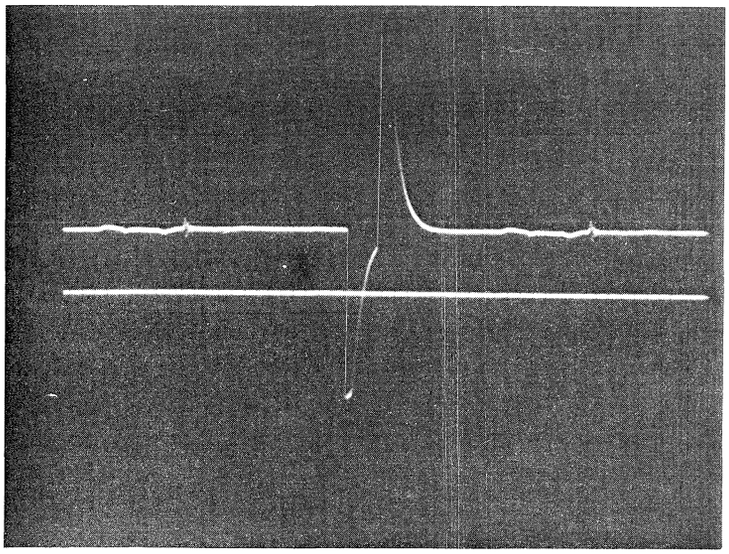


FIGURE 5 – Differentiated Line Sync Pulse

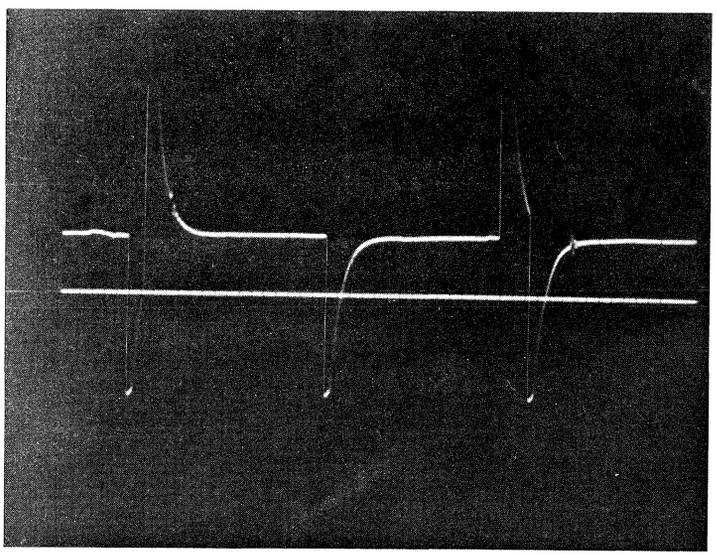


FIGURE 6 – Differentiation of Equalizing Pulse, Leading Edge of Field Sync Pulse and First Serrated Pulse

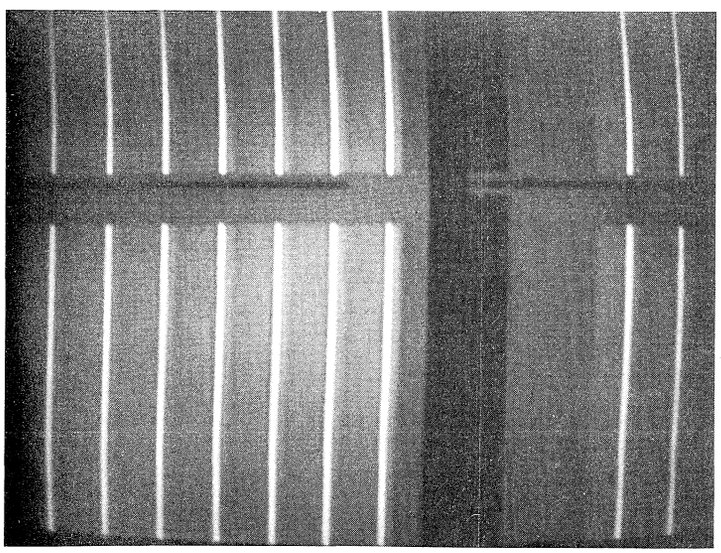
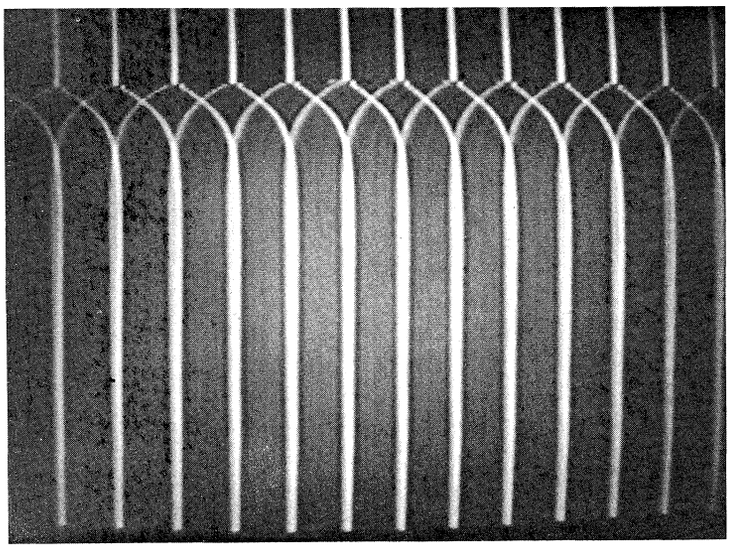


FIGURE 7 – Vertical Blanking Period With Differentiated Syncs

Typical APC Loop Transient Response
to 3 μs Sync Timing Delay



Transient Response When Sync Pulses
Are 2.3 μs Wide

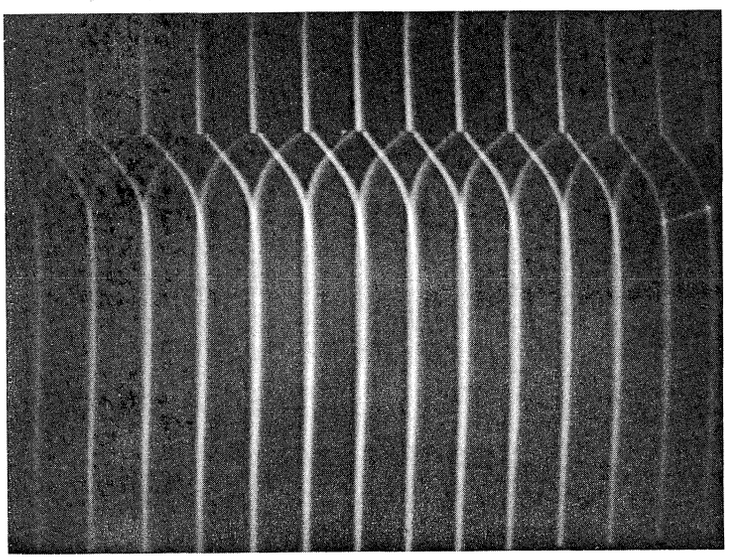


FIGURE 8 –

can be done by adding a dc offset to the phase detector sawtooth input such that the sync pulses become phase advanced with respect to the sawtooth, Figure 9 (see also Appendix B). For the MC1394, this can be done by placing a resistor between the sawtooth input (Pin 4) and ground. For a positive sawtooth input (MC1391) the resistor is connected to V_{CC}. The scope traces show the effect on the vertical blanking interval, and the effect of too much phase advance of the sync.

STATIC PHASING

Phase advancing the sync waveform with respect to the sawtooth raises the topic of proper static phasing of the APC loop. If there are no delays in either the video channel or the sync channel from the 2nd detector onward (if this is the point of sync take-off), then for proper static phasing the timing of the video at the picture tube cathode with respect to the sync flyback pulse will be that shown in Figure 10. To avoid folding the video on the raster, the video blanking period and the flyback pulse must be time co-incident, and since the sync pulse is not in the middle of the video blanking period it must be phase advanced with respect to the sawtooth reference waveform derived from the flyback pulse. Normally of course, in a color receiver, the video is delayed between the 2nd detector and the picture tube cathode to compensate for the reduced chroma channel bandwidth. This reduces the phase advance of the syncs with respect to the sawtooth to obtain proper picture phasing by 0.7 μs to 1.1 μs (depending on the quality of the chroma channel). However, if the syncs themselves are delayed – as can occur in sophisticated noise processing circuits – then the required

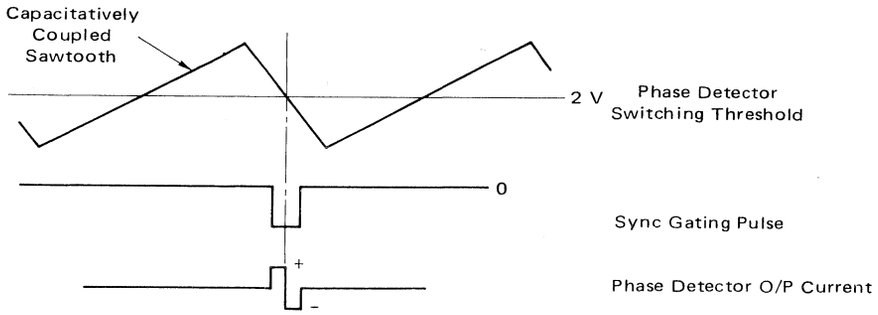


FIGURE 9a – Balanced Phase Detector Operation

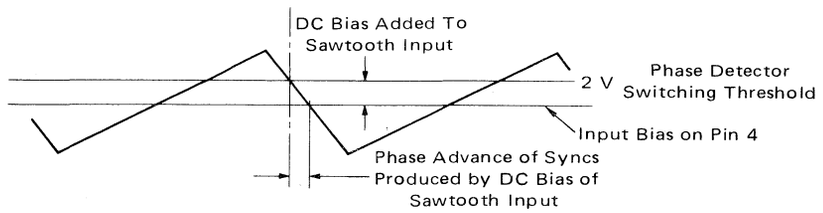


FIGURE 9b – Phase Detector Operation With DC Offset

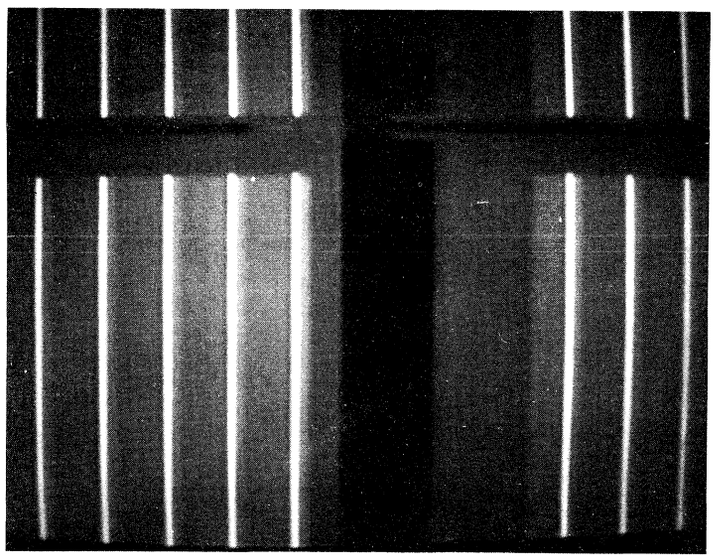


FIGURE 9c –
Compensating Top-Hook By Phase Advancing the Syncs With Respect to the Sawtooth

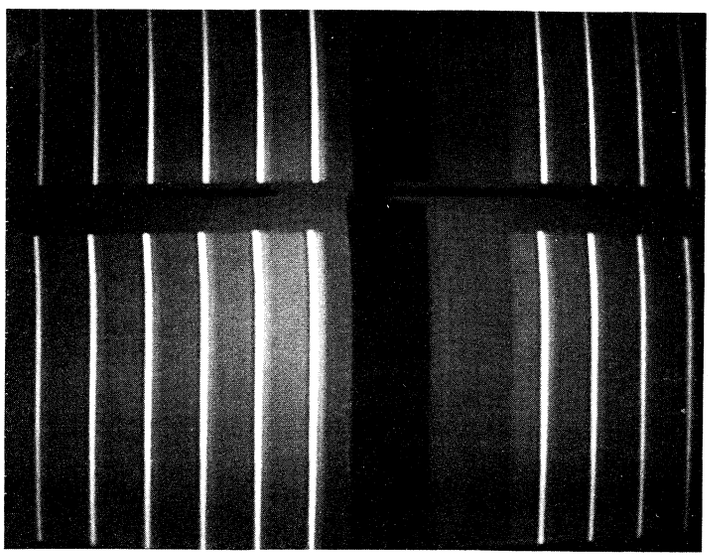
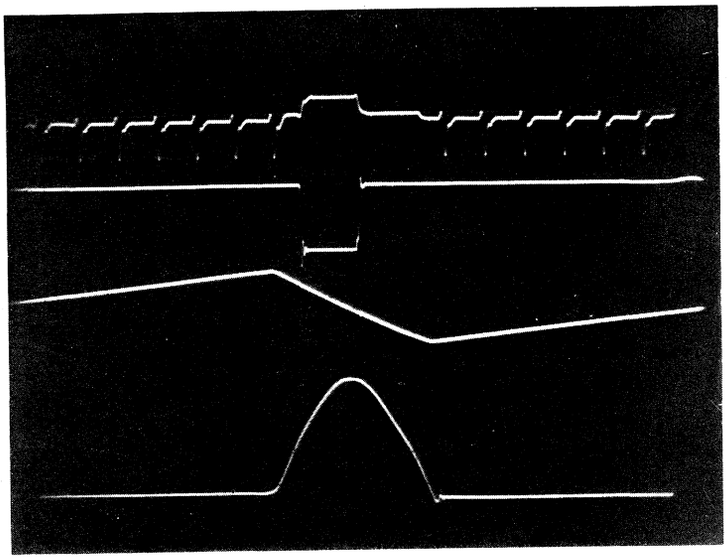


FIGURE 9d –
The Effect of Too Much Phase Advance of the Syncs



Video/Sweep Timing

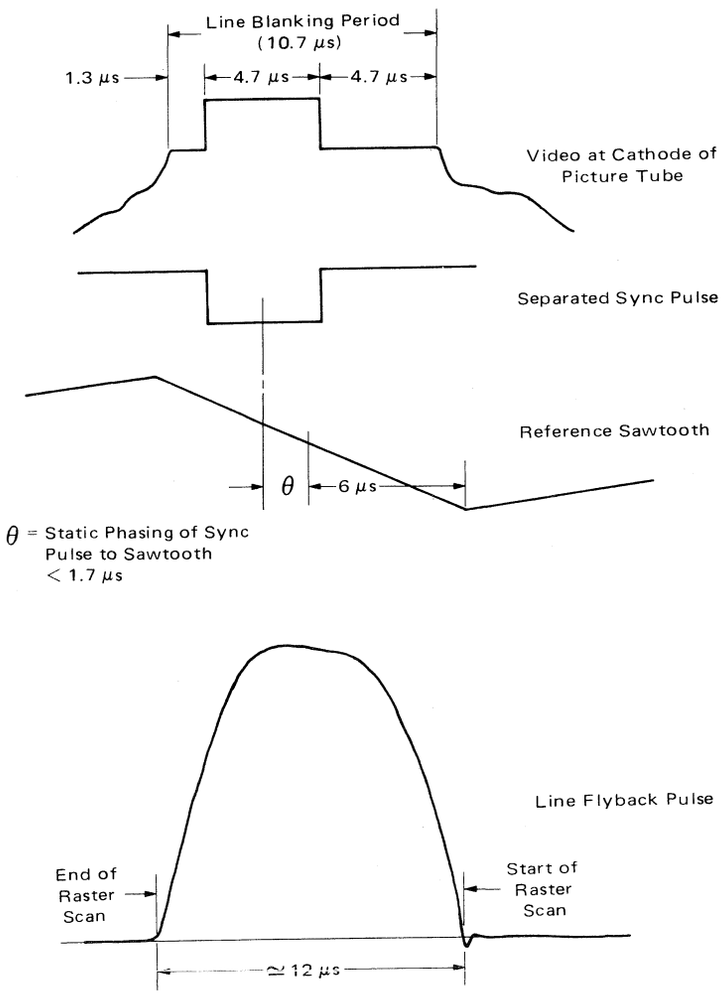


FIGURE 10 – Video/Sweep Timing with Picture Centered On Raster

phase advance is increased again and may be as much as 1.5 μs from the center of the sawtooth. Clearly, static phasing for an individual receiver design can modify the appearance of top-hook and a compromise may be necessary between ideal phasing and complete compensation of top-hook.

Rather like opening Pandora's Box, once we have accepted the idea of deliberate dc offsets to the phase detector to produce proper phasing and/or top-hook compensation, we now have a grapple with some of the undesirable aspects of offsets in the phase detector.

PHASE DETECTOR OFFSET

Under this heading comes related problems such as frequency push-out, asymmetry of pull-in and loss of synchronism during weak signal conditions, i.e., thermal noise conditions. Before discussing these topics in any detail, an important distinction must be made. Imbalances in the phase detector when the loop is synchronous are considered to be dc offsets. Their effect on the loop operation is to cause phase differences to exist between the sync and sawtooth waveforms – an obvious case is that mentioned above where an offset voltage is used to give proper static phasing of the picture on the raster. Imbalances that occur when the loop is asynchronous are considered to be ac offsets. Their effect is to modify the free-running frequency of the oscillator.

A convenient way to investigate offsets in a phase detector is to start out with a linear, balanced phase detector and a linear sawtooth waveform (a saw of good linearity is obtained from the circuits shown in Appendix C, where a capacitor is charged and discharged by constant current sources). With a power supply connected to the sawtooth input of the phase detector through a large resistor (Figure 11), the dc balance of the detector can be varied at will within the stable operating region. When the power supply is set to pull current from the sawtooth pin, the syncs become phase advanced with respect to the sawtooth. If the power supply gives current to the sawtooth pin, then the syncs become phase delayed.

If the phase detector is offset in each direction by small amounts (say 0.5 μs phase shift steps) and the pull-in range measured for each increase in phase shift, characteristics similar to those shown in Figure 12 will be obtained. While the syncs and sawtooth are centered and there is no imbalance in the phase detector, the pull-in range is equal on either side of f_H and is about ±300 Hz, the design center (equivalent to about 4 or 5 bars side-lock pull-in). As dc offsets are introduced to change the phasing, the pull-in range rapidly becomes asymmetrical until the point is reached when, although the oscillator is frequency adjusted on either side of f_H, pull-in actually occurs from one side only. 1/ Apparently, the oscillator is being "pushed out" from free-running at f_H. The reason for this is that with a linear sawtooth, introducing a dc offset into the phase detector for phasing purposes is also introducing an ac offset. It is this ac offset that causes the pull-in range to lack symmetry and, eventually, frequency push-out.

1/ Apparent pull-in from both sides will be obtained if the oscillator frequency is adjusted toward f_H while the syncs are applied, i.e., side-lock pull-in. However, when syncs are removed to measure the actual oscillator free-running frequency, this is found to be always on one side of the f_H. (The values plotted in Figure 8).

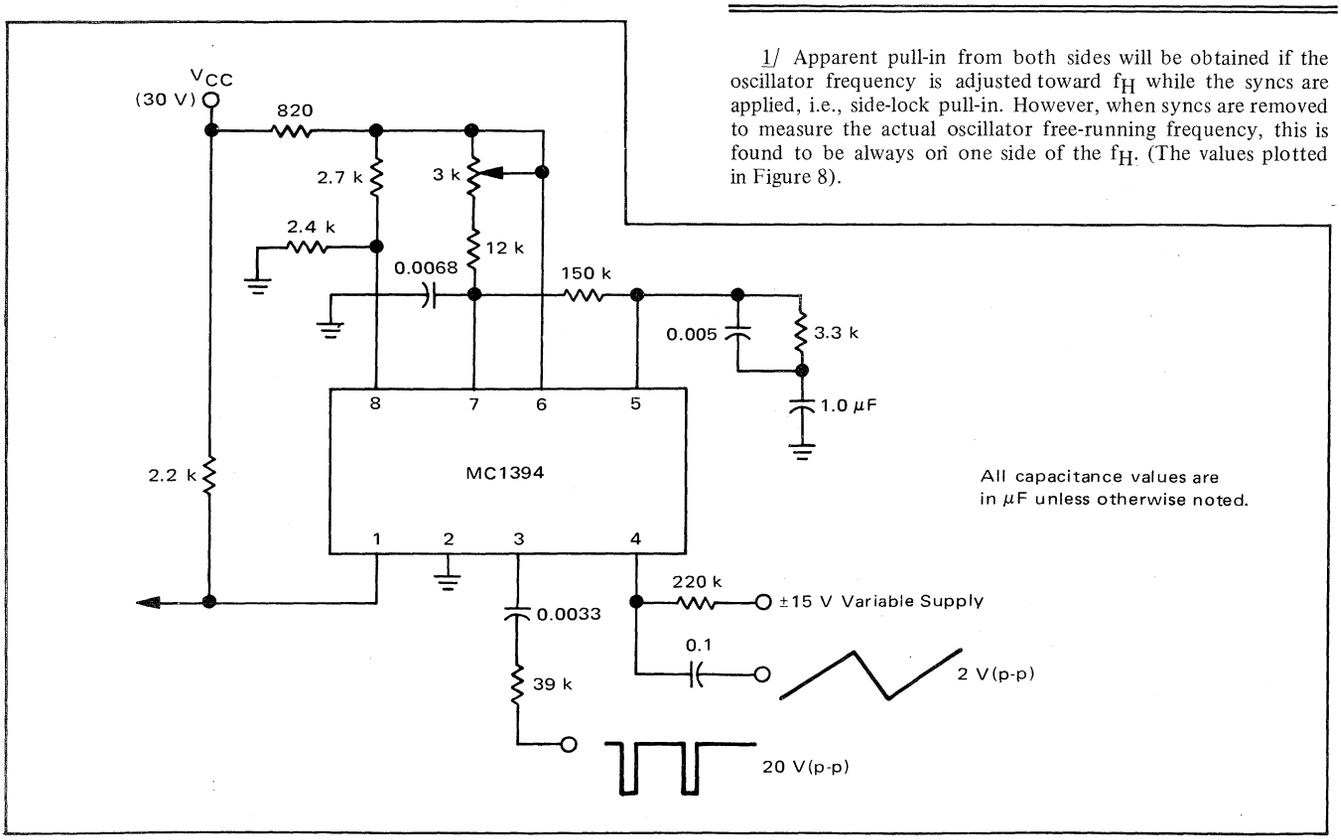


FIGURE 11 – Circuit for Imbalance Measurements

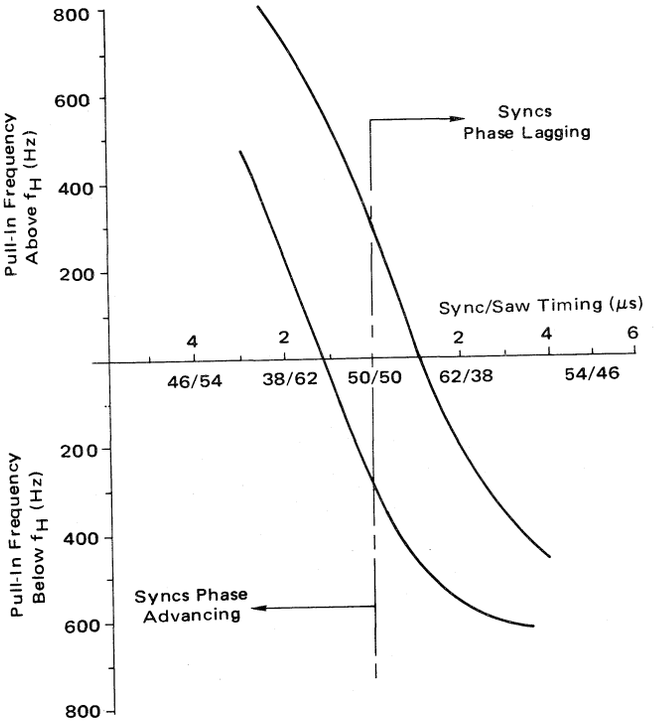


FIGURE 12 – Pull-In Range Versus Static Phasing

Referring back to Figure 9, it can be seen that a dc offset on the linear sawtooth pushes the switching point for the phase detector further up the sawtooth slope. When the loop is locked, the sync waveform will center on this point and the phase detector current to the oscillator is zero. Notice however, that the time for which the sawtooth voltage is above the phase detector switching threshold (during which time a gate pulse can produce a positive current from the phase detector) has become considerably less than the time for which the sawtooth voltage is below the phase detector switching threshold (when a gate pulse can produce a negative current into the phase detector). If the phase detector is being gated asynchronously under these conditions, there will be a mean negative current into the phase detector. An obvious example of asynchronous gating, of course, is during the pull-in process when the oscillator is off frequency. When the oscillator is off frequency and the loop is closed, a beat note with a dc component tries to pull the oscillator on frequency. The further off frequency the oscillator is, the smaller the dc component becomes, with a correspondingly weaker pull-in effect. When the oscillator is above f_H, the beat note lowers the oscillator frequency and, added to this, will be the mean negative current into the phase detector produced by the unequal duty cycle of the sawtooth about the switching threshold, also tending to lower the oscillator frequency. Thus, the pull-in effect above f_H is enhanced and that below f_H is decreased (Figure 12). Since the sawtooth is linear, the abscissa can be calibrated in terms of duty cycle rather than phase advance or delay of the syncs.

Another example of asynchronous gating is thermal noise at the sync input to the phase detector. If the oscillator is adjusted to f_H and the loop is closed, as the RF signal becomes weaker spikes of thermal noise will generate phase detector outputs. Since the detector can generate negative currents for a longer period than positive currents, the oscillator phase will shift as the thermal contamination increases 2/, and may reach the point that if the signal is momentarily interrupted, the oscillator will go out of lock (i.e., when the static phase shift > 0.5 μs). Thus, at weak signals the oscillator appears off frequency even though it was adjusted to f_H.

The need for a dc offset to the phase detector to achieve static phasing does not need to result in an ac offset. If the sawtooth waveform is made slightly nonlinear, the duty cycle about the switching threshold of the phase detector can be maintained at 50/50, even with the syncs phase advanced. The simple way to do this, when the saw is derived from a flyback pulse, is to shorten the integration time constant. This is an iterative process since this will also advance the static phasing slightly. Once proper phasing has been obtained, the sawtooth should be checked to see that the duty cycle is 50/50 at the switching point of the phase detector.

A word of warning: If the sawtooth slope is very steep in the vicinity of the switching point for the phase detector, small variations in dc offset will produce little noticable change in the static phasing. However, the change in duty cycle for the saw will be much larger and in the normal course of events, some asymmetry of pull-in is likely with any design.

FLAG WAVING

During the discussions on top-hook it was mentioned that sync-differentiation can lead to flag-waving. For example, if the coupling capacitor to Pin 3, the phase detector sync input, (Figure 11) is made much smaller and the sync source impedance is kept high at 39 kΩ, the Pin 3 waveform will appear as shown in Figure 13. During the increased duty cycle of the vertical sync pulse, the coupling capacitor becomes charged up to the input bias of Pin 3, and this turns off the phase detector until the vertical sync pulse has passed. Normally, the increased duty cycle of the vertical pulses results in the phase detector output current excursions shown in Figure 14. The upper trace is the even field vertical interval and lower trace the odd field. When the input capacitor charges up, the phase detector cuts off after about the first serration, and the output appears as shown in Figure 15. The output is now imbalanced between odd and even fields causing a phase offset that changes in polarity every field. The effect on the picture tube is shown in Figure 16, making vertical lines appear to bend first in one direction and then in the other.

2/ Note: This phase shift with thermal noise is a static phasing shift dependent on the ac balance of the phase detector. Dynamic phase errors, i.e., thermal jitter are still determined by the noise bandwidth of the loop (f_{NN}) and depend on the loop gain and filter characteristics.

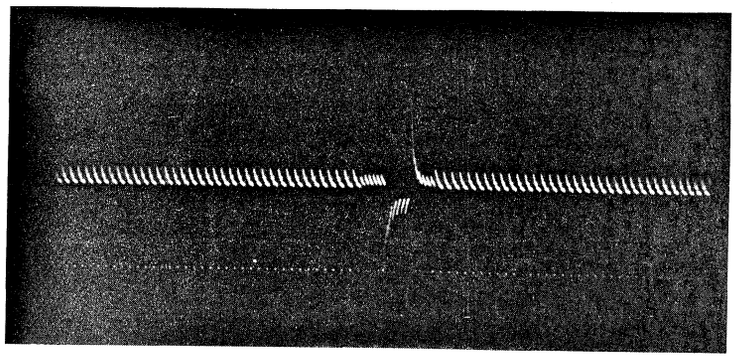


FIGURE 13 – Phase Detector Sync Input with Small Coupling Capacitor

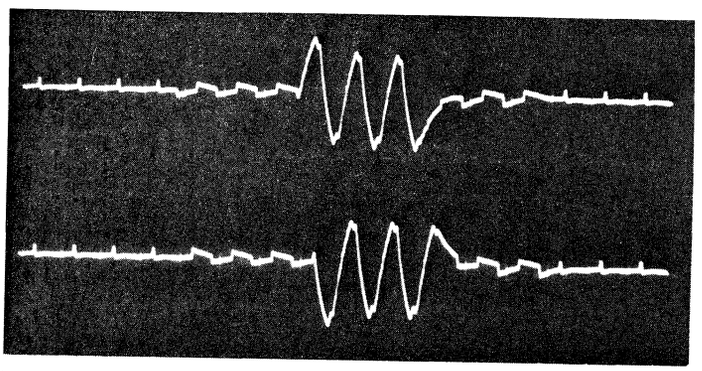


FIGURE 14 – Normal Phase Detector Output During Vertical Sync Pulse

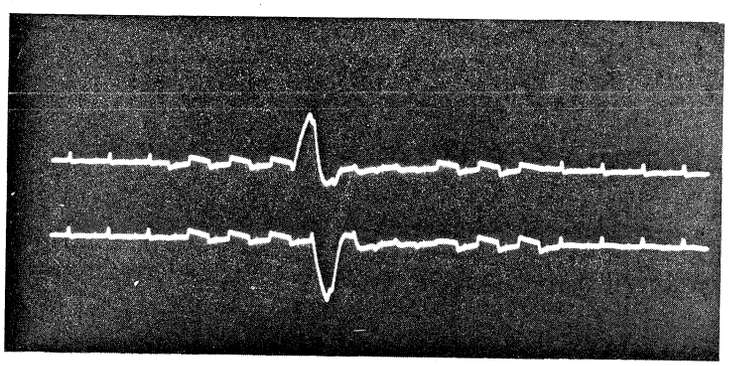


FIGURE 15 – Phase Detector Output With Sync Input of Figure 13

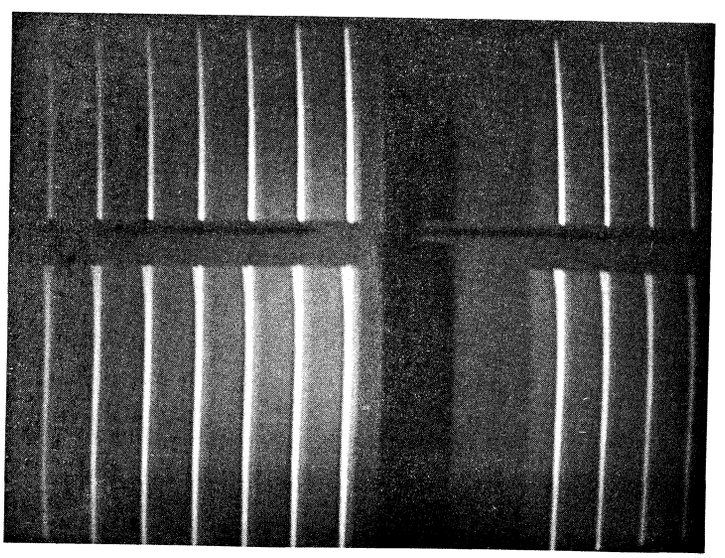


FIGURE 16 – Flag Waving of CRT

SUMMARY

This note has discussed some of the problems that can plague a horizontal APC loop design. Although the MC1394 has been used throughout as an example, the problems are general in nature and refer to many discrete designs. One final point, the discussion on detector imbalance assumed that a balanced detector was available. This need not be so, since the detector is usually deliberately unbalanced to effect phasing. Unless the intrinsic unbalance of a phase detector is subject to variation, it will be nullified in the phasing process.

REFERENCES

1. CER 110 – Horizontal APC/AFC Loops.
2. ibid, pp 6-7.

APPENDIX A

Television horizontal phase detectors have two regions of operation – a stable region and an unstable region (Figure A1).

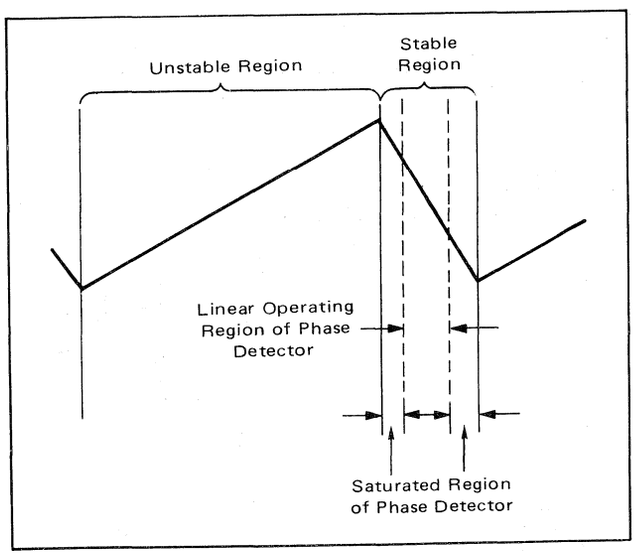


FIGURE A1

The stable region is usually confined to the steepest part of the reference sawtooth (i.e., $-dv/dt$ = max. for the MC1394) and the phase detector gain and polarity is always such as to correct phase errors. For the remainder of the sawtooth, or the unstable region, the loop gain is low and reversed in polarity. Frequently the phase detector output is not linear for the entire region of stable operation. The typical reactance control for an L-C oscillator usually saturates at the limits of the stable region and gated phase detectors saturate at the limits of the sync pulse width. The width of the linear region defines the hold-in range and the saturation current available outside the linear region controls the loop characteristics at the start of a large phase transient. As the sync pulse width is reduced, the mean charge current available for correction is decreased. When a phase transient takes the phase detector outside the linear region the speed of initial recovery will depend on the mean current available to charge the filter capacitors. The scope traces in Figure 8 show the effect of decreasing the sync pulse width and hence the mean charge current. The initial recovery speed is perceptibly slower resulting in a slightly longer total recovery time from 3 μs phase transient produced by the jitter generator. Once the recovery has reached the phase detector linear region, normal circuit operation resumes and the effects of reduced sync pulse width are negligible.

APPENDIX B

Figure 9a shows the timing between the sync and sawtooth inputs to the phase detector section of an MC1394. The sawtooth is linear enough that when it is coupled to the detector through a capacitor, the mid-point of the waveform will coincide with the dc input bias of the phase detector. This bias at Pin 4 (about 2 V) is the threshold level for the phase comparator and voltages above this will give a current output from the phase detector when it is gated on by the sync waveform. Voltages below 2 V will cause a current input to the phase detector. If the oscillator frequency is adjusted to f_H with the phase detector disconnected, then when syncs are applied and the loop is closed, the center of the sync will phase with respect to the sawtooth to produce a net zero output from the phase detector. To change the phasing, the comparator can be offset by adding a resistor to ground from Pin 4, and the syncs will advance in phase until the phase detector net output is again zero, Figure 9b. It is not necessary to add a resistor to Pin 4 to change the phasing. If the sawtooth is non-linear, this will change the relative phasing of the sync and sawtooth waveforms (Figure B1 and B2). For integration time constants (RC) too short to produce linear sawtooths, phase advance of the sync pulse will be obtained. If some of the flyback pulse is added directly to the sawtooth (through R1), this will also cause the sync pulse to advance in phase.

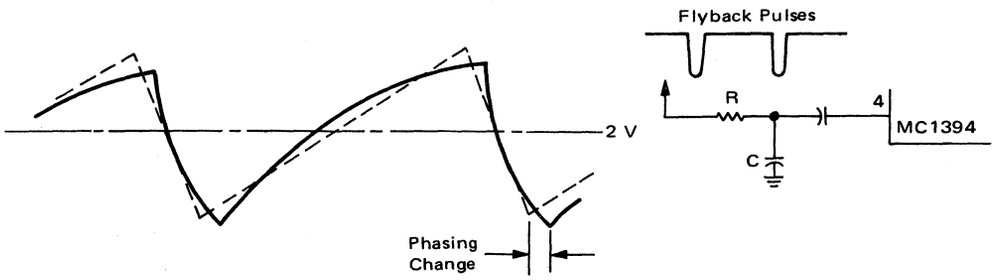
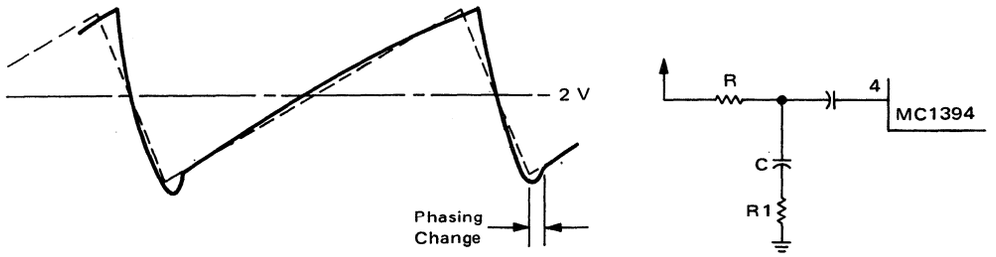


FIGURE B1 – Pin 4 Waveform



*Note: Usually adequate phasing cannot be achieved entirely by these methods without introducing other problems (see discussion of ac imbalance)

FIGURE B2 – Pin 4 Waveform

APPENDIX C

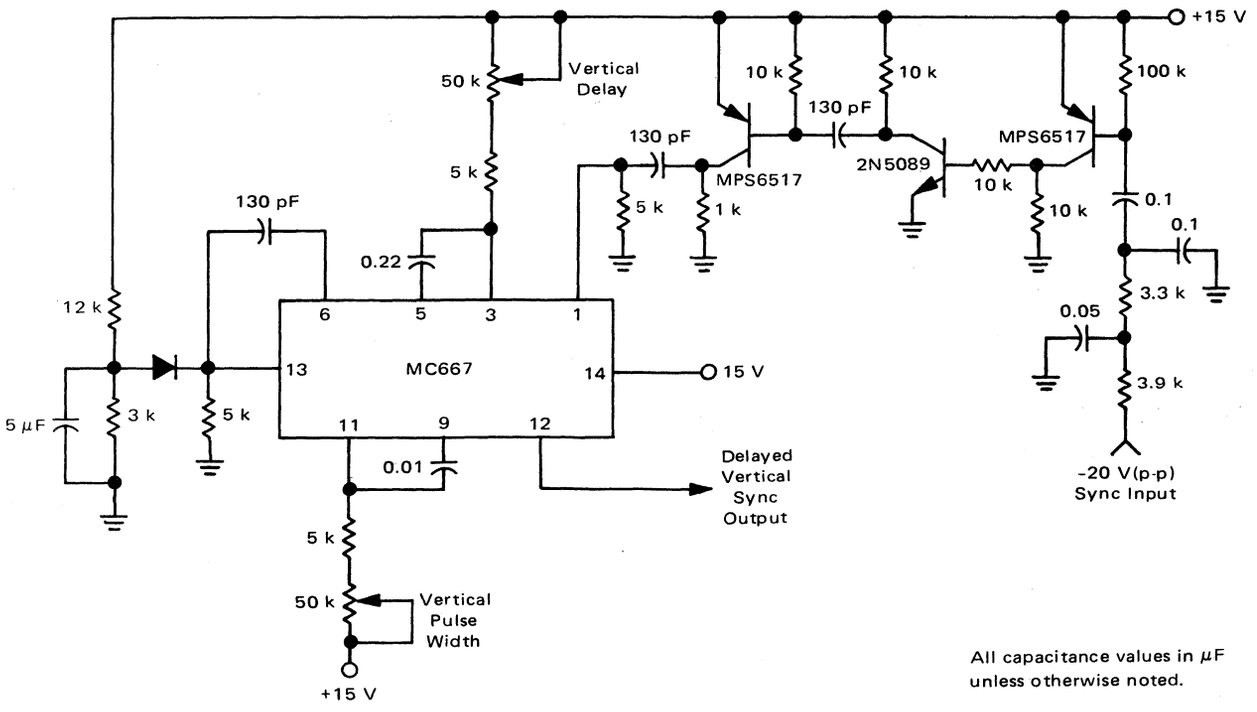


FIGURE C1 – Vertical Sync Delay Circuit

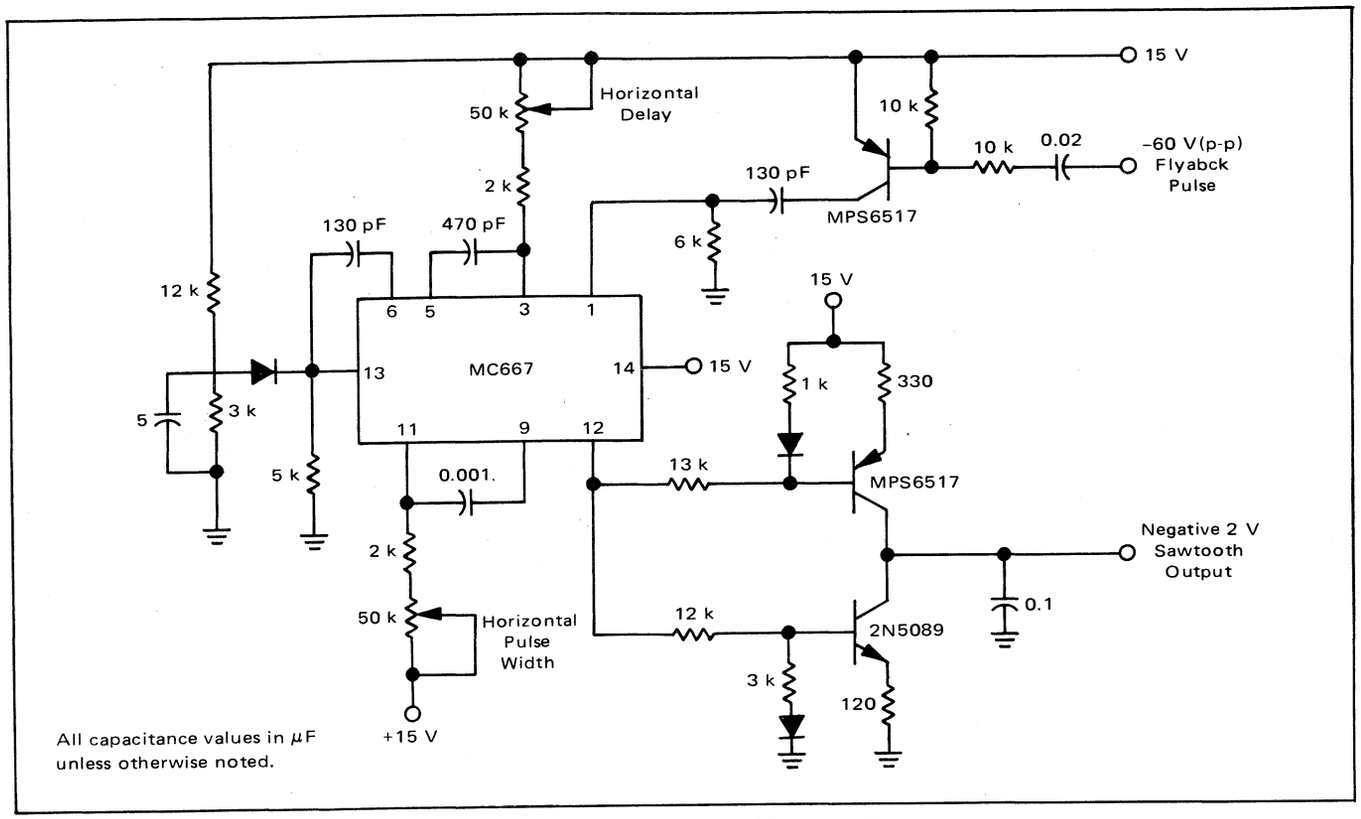


FIGURE C2 – Delayed Horizontal Sawtooth Circuit

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